GUEST EDITORIAL PREFACE

Special Issue on Networked Embedded Systems

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The research articles in this special issue address some of the challenges of on-chip networked embedded systems and low-power distributed wireless embedded systems usually termed as wireless sensor networks. These networked embedded systems have potential for far-reaching societal advancements.

High-performance video/audio processing, medical applications, networking services, scientific computing and hybrid computing of various applications require enormous computing capacity which can be realized using multicore embedded systems. Network-on-Chip (NoC) is generic and scalable communication architecture for many core systems. A number of different NoC architectures along with frameworks and tools for high-level exploration of NoC architectures have been proposed during this decade. Also, many NoC architectures have been implemented and evaluated in both FPGA and ASIC platforms. Most of existing approaches either provide exploration and design solutions without taking rapid prototyping into account, or provide rapid prototyping without exploration. There is a need to bridge this gap by developing EDA tool flow which performs high-level exploration, automatic RTL implementations of the interconnection network and rapid prototyping. Technology scaling has brought about dramatic rises in the on-chip power density of modern microprocessors. Higher temperatures or uneven distribution of temperatures result in timing uncertainties which causes performance and reliability problems. Three-dimensional (3D) stacking of chips offers greater device integration as well as flexibility, besides reduced signal delay and interconnect power. However, 3D stacking also exacerbates the on-chip thermal issues and increases packaging and cooling costs. In order to resolve these issues, and avoid high and uneven temperatures, accurate thermal modeling, and analysis, as well as thermal-aware mapping algorithms and placement optimizations are crucial.

The number of applications which can take advantage of wireless sensor networks (WSN) is tremendous. More and more applications are

emerging to solve several problems in data acquisition and control in different environments, taking advantage of this technology. In this context, hardware design of the sensor network node becomes critical to satisfy the hard constraints imposed by wireless sensor networks, such as low power consumption, low size and low cost. While WSN system software and protocols have been in constant evolution since the debut of this technology, hardware embedded architectures suited for WSN have not evolved along with their software counterparts. This lack of evolution in the WSN nodes' architecture leads to rising difficulties on meeting the strict energy requirements of increasingly demanding applications. The architectures are not prepared to include upgrades such as new energy management modules or even more energy efficient communication units. The challenges most often associated with WSN design is that sensor nodes operate with limited energy budgets. Typically, they are powered through batteries, which must be either replaced or recharged when depleted. For some nodes, neither option is appropriate due to environmental or cost constraints. In this case, harvesting energy from the surrounding environment is the most promising alternative.

This special issue on Networked Embedded Systems presents six articles which address some of the key issues discussed above. Four of the papers addresses issues for high-performance NoC based many core systems and the other two focuses on solution for low-power networked embedded systems. In the former category, two of the four articles deal with a more generic design approach for NoC (design flow and architecture) and the rest two present thermal issues in 2D and 3D stacked systems. A modular platform for WSN nodes and smart energy harvesting technique are proposed in the later group of papers.

The research article "*A novel prototyping and Evaluation framework for NoC-based MPSoC*" presents a novel EDA tool flow which carries out high-level exploration, automatic RTL implementation of the interconnection network and rapid prototyping. The flow performs high-level design exploration and selects the optimal NoC topology and application mapping, given a set of design constraints and goals. From the selected topology, the proposed flow automatically generates the corresponding NoC RTL code, testbenches for RTL verification, as well as the appropriate files for rapid prototyping in Xilinx FPGA devices. This greatly speeds up the design, verification and prototyping process, and hence the Non Recurring engineering cost. Furthermore, the automation of the RTL design and rapid prototyping hides many low-level implementation details from the designer, while still allowing the designer to control NoC parameters or optimize them for specific metrics such as performance, power consumption and area. The paper "*Cluster based Networks-on-Chip: An Efficient and Fault-Tolerant Architecture using Network Interface Assisted Routing*" proposes an efficient and reliable network interface assisted routing strategy for partial virtual channel sharing based NoC architecture. The proposed routing strategy along with the specified architecture is able to recover the Processing Element (PE) disconnected from the network due to network level faults by allowing the PE to transmit and receive the packets through the other router in the cluster.

One of the two articles addressing thermal challenges is "*Exploration of Temperature Constraints for Thermal-Aware Mapping of 3D Networks-on-Chip*". In this work, three integer linear programming (ILP)-based static thermal-aware mapping algorithms are proposed in order to examine the thermal constraints in 3D NoC. Based on complexity analysis, only two of the algorithms are chosen and developed further and their proficiency is examined. According to the exploration, power balancing early in the mapping algorithm does not affect chip temperature. In addition, taking into account the explicit performance constraints in the thermal mapping has no major effect on performance. The second thermal related paper is "*Exploration of Temperature-Aware Placement Approaches in 2D and 3D Stacked Systems*". This paper presents an exploration of temperature-aware placement approaches in

both 2D and 3D stacked systems. The authors developed various thermal models to investigate the effect of uniform power distribution, thermal-aware placement in 2D chips and 3D stacked systems on the thermal performance of the system thereby providing with metrics which can be used for thermal-aware mapping. The metrics obtained in this parametric study provides thermal guidance for circuit designers on optimizing the die layout from the thermal perspective for various thermal parameters.

The remaining two articles of this special issue propose solution for power efficient wireless sensor network's nodes implementations and both papers are written by the same research group and complement each other. The authors of "*MoteIST: A Modular Low-Power Approach to Wireless Sensor Networks Nodes*" article proposes a platform called MoteIST which introduce higher modularity of nodes and address the energy management issues while maintaining compatibility with previously designed software and sensing boards. This platform allows implementation of different energy efficient strategies, including energy harvesting modules and different power saving communication units. In "*Smart Ultra Low Power Energy Harvesting System*" paper the authors proposes design of a power supply which harvests energy from its environment. This supply not only can work with multiple energy sources but also can extract the maximum possible energy from them. It can also provide important information concerning the energy resources of the system.

We are thankful to the authors for their research contributions. We would also like to acknowledge the support we got from a wonderful review team which provided timely, extensive and constructive feedbacks to the contributing authors as well as the Guest Editors. We hope that these papers widen the horizon of researchers as well as developers of networked embedded systems and open additional platforms for further investigation into this inexhaustible and interesting field.

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